

Lab 2 - 7 Segment Display Decoder Circuit Design.

Student: _____

In this lab we will build a decoder circuit that can drive a common anode 7-segment LED display using a combinational logic circuit. The logic circuit is designed with four inputs and seven outputs. The four inputs will be connected to the switches on the Basys 3 development board, while the seven outputs will be connected to one of the four common anode 7-segment LED displays on the development board. Using Karnaugh's map, logic circuitry for each input to the display will be designed. Figure1 shows a common anode 7-segment LED display and the pinout of the Basys 3 development board.

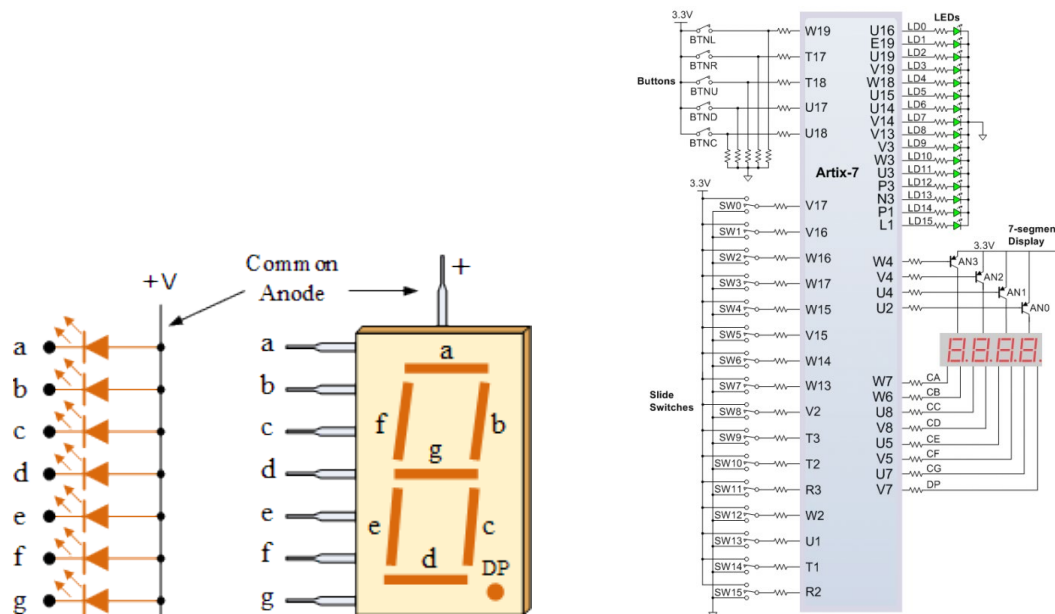


Figure 1

Table 1 shows the truth table of a binary-coded decimal (BCD) to seven-segment decoder with common anode display. The truth table has 7 different output columns corresponding to each of the 7 segments. A 0 will turn on a segment because they are 7 segment displays. Inputs 10-15 are not used so the outputs are all X for these outputs as we don't care what they are.

Digit	Inputs				Outputs						
	A	B	C	D	CA	CB	CC	CD	CE	CF	CG
0	0	0	0	0	0	0	0	0	0	0	1
1	0	0	0	1	1	0	0	1	1	1	1
2	0	0	1	0	0	0	1	0	0	1	0
3	0	0	1	1	0	0	0	0	1	1	0
4	0	1	0	0	1	0	0	1	1	0	0
5	0	1	0	1	0	1	0	0	1	0	0
6	0	1	1	0	0	1	0	0	0	0	0
7	0	1	1	1	0	0	0	1	1	1	1
8	1	0	0	0	0	0	0	0	0	0	0
9	1	0	0	1	0	0	0	1	1	0	0
10	1	0	1	0	x	x	x	x	x	x	x
11	1	0	1	1	x	x	x	x	x	x	x
12	1	1	0	0	x	x	x	x	x	x	x
13	1	1	0	1	x	x	x	x	x	x	x
14	1	1	1	0	x	x	x	x	x	x	x
15	1	1	1	1	x	x	x	x	x	x	x

Table 1

Step 1 Simplify the logic for each of the seven outputs using a Karnaugh map. For each output, place all the 1's and X's from the table into its Karnaugh map and make sure that all the 1s are put into the biggest group they can be put in. You only have to use the Xs if they help make put the 1s in bigger groups as this will simply the logic more. Write out the sum of products for each group.

CD \ AB	00	01	11	10
00				
01				
11				
10				

CA =

CD \ AB	00	01	11	10
00				
01				
11				
10				

CB =

CD \ AB	00	01	11	10
00				
01				
11				
10				

CC =

CD \ AB	00	01	11	10
00				
01				
11				
10				

CD =

CD \ AB	00	01	11	10
00				
01				
11				
10				

CE =

CD \ AB	00	01	11	10
00				
01				
11				
10				

CF =

CD \ AB	00	01	11	10
00				
01				
11				
10				

CG =

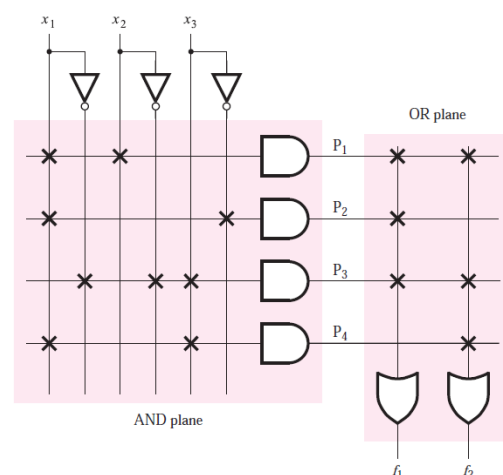


Figure 2

Step 2 Draw a combinational logic circuit for each output signal. The circuit will have 4 inputs (A, B, C, D) and 7 outputs (CA, CB, CC, CD, CE, CF, CG). The circuit in figure 2 is an example of a circuit with 3 inputs (X_1, X_2, X_3) and 2 outputs (f_1, f_2).

Step 3 Implement the 7 Segment display decoder circuit in VHDL. Copy steps A and B from lab 1 to create a new project and add a design file for your circuit. The design file should have the same name as your first name. Your decoder circuit should have 4 inputs A, B, C, D and 7 outputs CA, CB, CC, CD, CE, CF and CG. Insert your VHDL code in the text box below.

Step 4 Copy steps C and D from lab 1 to implement a test bench for the 7 Segment display decoder circuit using VHDL. Your testbench will check that all 10 valid input combinations for inputs A, B, C and D are working correctly. These 10 valid input combinations range from “0000” to “1001”. The testbench should also check that the decoder returns the correct values, the output values for CA, CB, CC, CD, CE, CF and CG should be 0, 0, 0, 0, 0, 0, 1 for example when the inputs for A, B, C and D are 0, 0, 0, 0 as shown below. Insert your VHDL code for your testbench in the box below.

```
A <= '0';
B <= '0';
C <= '0';
D <= '0';
wait for 1 ns;
if (CA = '0') and (CB = '0') and (CC = '0') and (CD = '0') and (CE = '0') and (CF = '0') and (CG = '1') then
report "pass for inputs 0000"; else
report "failed for inputs 0000"; end if;
```

Take a screengrab of your waveform and insert it in the box below.

Insert the pass fail messages from your testbench in the box below.

Step 5 Copy step F from lab 1 and create a constraints file for the 7 Segment display decoder circuit. The constraints file should connect the inputs to the switches on the Basys 3 development board, connecting input A to SW3, B to SW2, C to SW1 and D to SW0. The constraints file should also connect the outputs CA, CB, CC, CD, CE, CF and CG to segments CA, CB, CC, CD, CE, CF and CG on the 7 Segment displays. Figure 1 shows what pins connect the FPGA to the switches and 7 Segment display. Paste your code for the constraints file in the box below.

Step 6 Copy step G from lab 1 to generate a bitstream for your design that could be downloaded onto the Basys 3 development board. Insert a screengrab of the schematic for your design and input/output list in the box below to show that the bitstream was generated successfully. Step H from lab 1 describes how to do this.